

Scanning Capacitance Microscopy (SCM)

High Resolution and High Sensitivity Imaging of Charge Distribution

Characterization of Semiconductor Device with Non-Destructive Technique and High Spatial Resolution

Physical characterization of semiconductor device has always been a challenging task for device engineers and researchers. Up to now, standard methods for characterizing semiconductors did not provide an effective means for determining two-dimensional quantities of sub-device scale. These methods include Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), Secondary Ion Mass Spectroscopy (SIMS), Spreading Sheet Resistance Profiling (SRP), and one-dimensional Capacitance Voltage (C-V), etc. With the advent of smaller device geometry and high reliability requirements, new characterization tools are needed. As alternative approaching tools, various types of scanning probe microscopy (SPM) have been applied to not only characterizing semiconductor devices but also monitoring semiconductor device processes. Scanning Capacitance Microscopy (SCM) combined with Atomic Force Microscopy (AFM) is one of the powerful methods for the characterization of semiconductor devices due to its non-destructive technique and high spatial resolution.

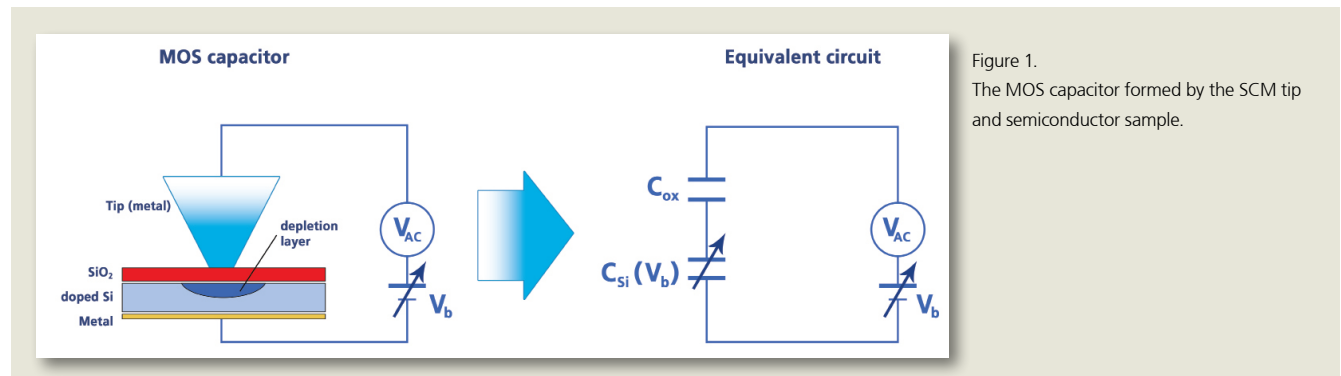


Figure 1. The MOS capacitor formed by the SCM tip and semiconductor sample.

Scanning Capacitance Microscopy (SCM) of the XE-series AFM images spatial variations in capacitance. One of the most common applications of SCM is mapping of the carrier concentration on the non-uniformly doped samples. For example, determining dopant profiles in ion implanted semiconductors, characterizing the electrical properties of the gate oxide in Metal-Oxide-Semiconductor (MOS) devices, and mapping defect distribution can be successfully achieved by the SCM. The SCM can be also used in the field of non-volatile ultrahigh density memory application.

The SCM consists of a conductive metal probe tip and a highly sensitive capacitance sensor in addition to the normal AFM components. Like EFM, SCM applies a voltage between the tip and the sample as in MOS structures. The metallic probe tip in contact with the oxidized semiconductor sample forms a MOS capacitor. The MOS capacitor has two capacitors in series: one is from the insulating oxide layer and the other from the active depletion layer near the oxide/silicon interface. Figure 1 depicts the MOS capacitor formed by the SCM tip and the semiconductor. The total capacitance is determined by the oxide thickness and the thickness of depletion layer which depends on the carrier concentration in the silicon substrate and the applied DC voltage between the tip and the semiconductor.

Figure 2 shows DC bias dependence of the capacitance and the differential capacitance, respectively. Figure 2 (a) shows a typical high frequency capacitance-voltage (C-V) curve for p-type and n-type semiconductor samples. Low carrier concentration corresponds to relatively high peak amplitude in the differential capacitance. The applied DC bias voltage changes depletion width in the silicon. In addition, AC bias voltage produces capacitance variation at the depletion edge at fixed DC bias.

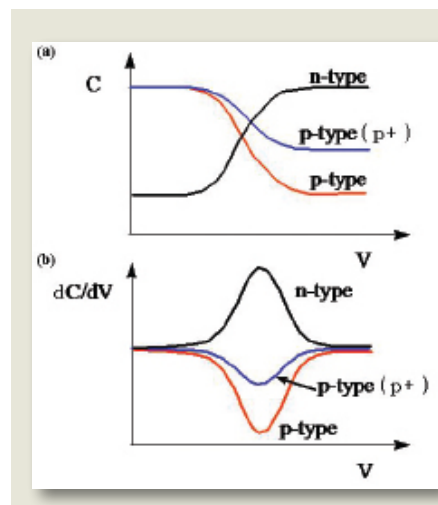
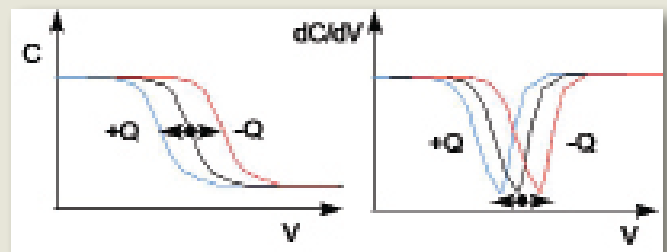


Figure 2. DC bias dependence of (a) the capacitance and (b) the differential capacitance for both n-type and p-type.

Figure 3. Positively and negatively trapped charges in the insulator on the semiconductor cause a parallel shift in high-frequency C-V and dC/dV curve along the voltage axis.



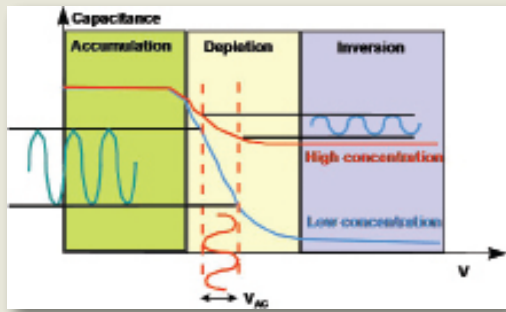


Figure 4. The detection scheme of dC/dV measurement for a p-type semiconductor sample.

Trapped charges in the insulator of a semi-conductor cause a parallel shift in high-frequency C-V curve along the voltage axis. Figure 3 indicates that positively and negatively trapped charges cause the C-V and the dC/dV curve to shift left and right, respectively. At zero bias, the capacitance and the dC/dV value in the case of charged state are different from that of uncharged state.

Figure 4 describes the detection scheme of dC/dV measurement for a p-type semiconductor sample. The applied AC bias voltage produces capacitance variation at fixed DC bias. A lock-in amplifier can detect the variation of the amplitude and the phase in capacitance signal at the same frequency of the applied AC voltage at the particular DC bias voltage. Thus the lock-in output is proportional, not to the capacitance, but to the slope of the C-V curve at the particular DC bias. Therefore the lock-in output is equivalent to the differential capacitance (dC/dV). The SCM detects differential capacitance at fixed DC and AC bias voltage as the tip moves across different regions in carrier concentration.

In Figure 5(a), the operational mechanism of the capacitance measurement for the XE-series SCM is shown. The capacitance sensor adopts an RF (~1 GHz) oscillator couples a resonator with the RF power detection circuit.

Figure 5. (a) Schematic diagram of the XE-series SCM. (b) A change in the tip-sample capacitance.

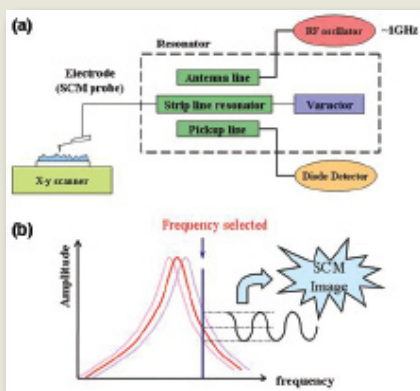
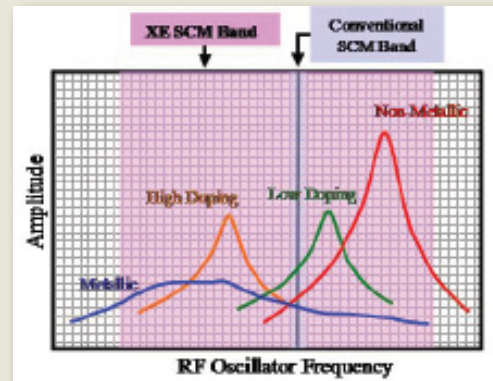


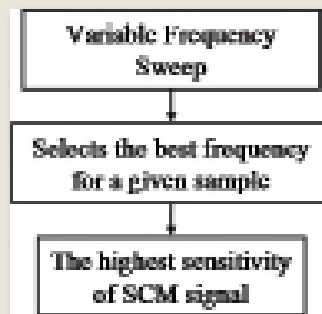
Figure 6. Comparison of XE SCM band (red) and conventional SCM band (blue). Resonance curves of different materials are plotted as a reference.



The resonator comprises a resonance circuitry along with the probe and the sample. A change in the tip-sample capacitance changes the resonance characteristic of the resonator, which results in the difference of the amplitude of the voltage output from the diode detector.

In Figure 6, SCM resonance curves of different samples are shown. The shape and the position of the resonance curve varies with different materials. For example, the resonance frequencies of metals are relatively low while those of dielectrics are relatively high. Note that the resonance frequency is not the only factor changing with various materials; quality factor of each curve also varies from about 35 to 40. As conventional SCM uses an RF oscillator with a fixed operating frequency, a good SCM image of metallic and dielectric samples are hard to obtain. As the point of measurement is fixed, the position of maximum sensitivity can hardly be maintained. When the resonance curve of a sample moves away from the operating frequency, the SCM image must be taken with a lower sensitivity or the resonance curve must be moved back to a better operating position by the means of blind rearrangement of measuring environments. Therefore, the structure of the conventional SCM sensor becomes the critical bottleneck, which limits the SCM application.

Figure 7. The advantage of high resolution and high sensitivity XE SCM imaging with variable operating frequency SCM probe.



The XE-series SCM, as shown in Figure 7, is operated with a highly sensitive and a high spatial resolution SCM probe in conjunction with a tunable operating frequency to select the optimal resonance frequency and quality factor for each measurements. In addition, the innovative electrical shielding, as shown in Figure 8, and dielectric probe holder of the SCM probe allows for measurements free of environmental effect. This low dielectric material reduces stray capacitance and increases the S/N ratio.

Figure 9 shows the schematic diagram of the advanced SCM probe used in the XE-series SCM. The SCM probe is connected to a microwave resonator, which has an internal variable capacitor, with which one can adjust the probe to have an optimum resonance frequency (f_r) and quality factor (Q). VCO provides excellent frequency stability and makes advanced modes possible such as frequency sweep. Sensitivity is proportional to $1/\sqrt{BW}$ and, therefore, higher frequency provides higher sensitivity.

The SCM probe with variable operating frequency covers a wide RF band of 160MHz from 890 MHz to 1050 MHz. From the resonance curve acquired, one can maximize the resolution and sensitivity of the SCM probe by choosing the operating frequency which is at the maximum slope as exemplified in Figure 5. If the resonance curve has a shoulder peak in either left or right of the center peak, one should choose a point apart from the shoulder to prevent non-linearity in the output signal.

As the SCM sensor operates within the RF range, the electro-magnetic radiation from the resonator to the metallic structures in vicinity causes stray capacitance. Therefore, the unnecessary radiation should be minimized through proper insulating and shielding. For this reason, we avoided metallic materials for the mechanical parts in the vicinity of the probe, and ceramic material was used instead. Also the length of the wiring from the SCM resonator to the probe was minimized, and the size of the opening at the front of the resonator was optimized.

Figure 8. XE SCM probe with variable operating frequency. The probe is completely shielded to minimize stray capacitance.

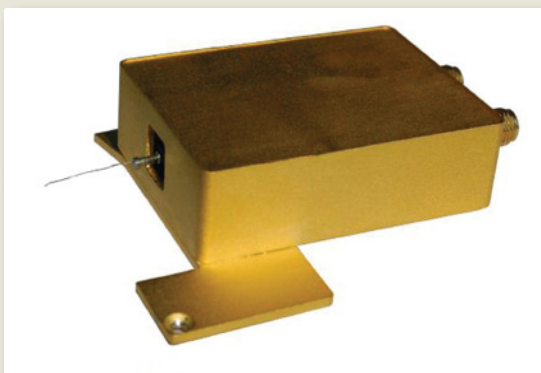
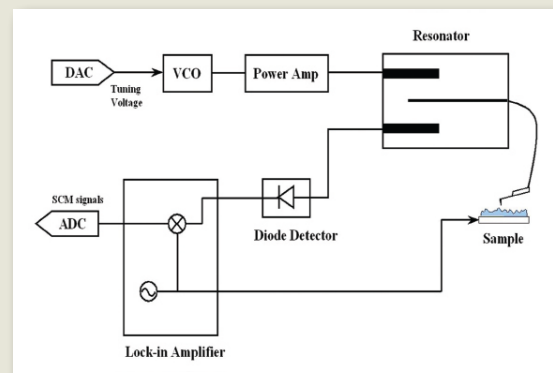


Figure 9. The schematic diagram of the XE SCM probe with variable operating frequency.



One of the most common applications of the XE-series SCM is mapping of the carrier concentration on a non-uniformly doped semiconductor sample. Up until now, conventional tools such as SIMS, SRP, and one-dimensional C-V provided dopant or carrier concentration information with very high accuracy and resolution limited in only one-dimension. Thus quantitative two-dimensional information could be inferred from one-dimensional measurements. However, the XE-series SCM has shown great potential for direct measurements of two-dimensional activated carrier concentration with nanometer scale accuracy.

Figure 10. The comparison of ion implanted Si sample imaging by XE SCM (left) and conventional SCM.

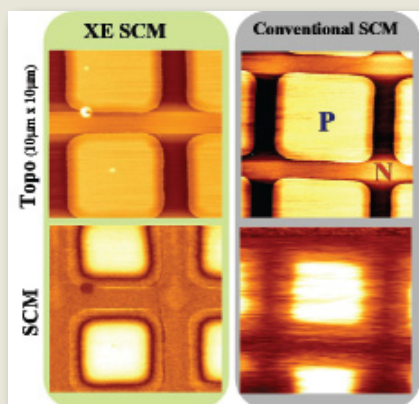


Figure 11. (a) The topography and (b) the SCM image of the semiconductor surface. The bright region in the topography image represents a thermally grown silicon dioxide pattern with 70 nm height. The bright circular and rounded rectangular regions in the SCM image are heavily doped by As+ ion with having 50 keV energy and 1014 ions/cm2 dose density.

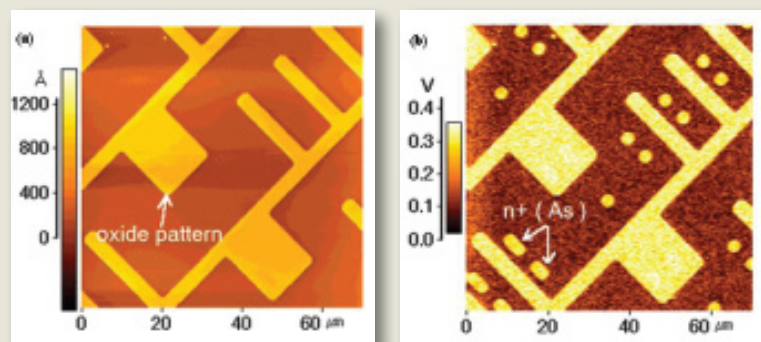
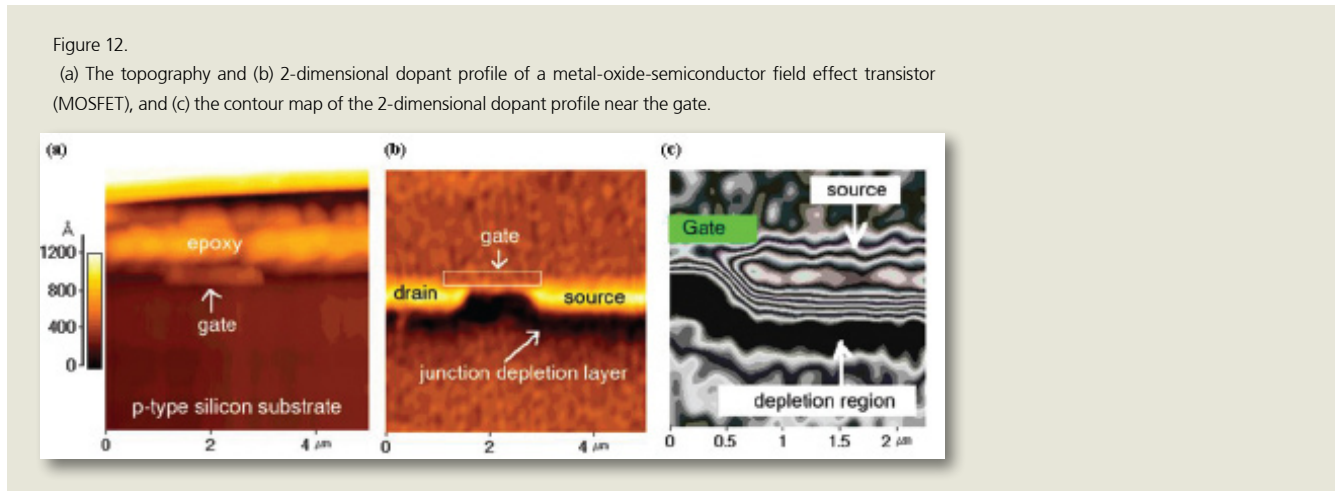


Figure 11 shows the topography and the SCM image of a semiconductor surface. The bright region in the topographic data represents a thermally grown silicon dioxide pattern of 70 nm height. The XE SCM visualizes and determines the impurity concentration and variation in oxide thickness on the surface. Bright circular and rounded rectangular regions in the SCM image are heavily doped by As⁺ ion of 50 keV energy and 10¹⁴ ions/cm² dose density. Bright contrast at the patterned oxide region in SCM image indicates that capacitance variation for AC voltage swing (dC/dV) is very small, such as in the heavily doped region due to the thick oxide layer. Therefore this result indicates that SCM can measure relative variations in the insulator thicknesses.

Figure 12(a) and (b) show the topography and the 2-dimensional dopant profile of a Metal-Oxide-Semiconductor field effect transistor (MOSFET), respectively. Figure 12(c) is the contour map of Figure 12(b) near the gate. Highly doped source, drain and junction depletion region can be successfully visualized by the XE SCM, but these regions can not be seen in the AFM topography images. Also there are no measurement tools to determine the junction depletion layer at the p-n junction edge.



As another usage, the XE SCM can be used for the characterization of gate oxide in MOS devices. As the gate oxide gets thinner, problems and failures can occur by trapped charge in the oxide during device operation. At present there are no tools to find the local failure and generated electrical defects. However, the XE SCM can carry out mapping of localized charges and defects in the insulator with a nanometer resolution.

The XE SCM can also be used in the field of ultrahigh density non-volatile semiconductor memory. Stored charges in the insulator layer of the Metal-Insulator-Oxide-Semiconductor (MOS) hetero-structure non-volatile memory can be readout by the XE SCM. In 1991, Barrett and Quate demonstrated a SCM based ultrahigh density data storage for Metal-Nitride-Oxide-Silicon (MNOS) system.

In Figure 13, the direct imaging of charge redistribution with XE SCM is illustrated, where the charge is trapped by a voltage stress on the surface of a 6 nm thick SiO₂ on P doped Si. The seconds below each image denotes the time after the initial stress of 60 seconds with 9.5 V applied.

Figure 14 shows the charge distributions written on a thin silicon dioxide. By applying a voltage pulse at specific location of the letters, "PSIA and underline", charges are trapped in the silicon dioxide, a thin insulator. As clearly demonstrated below, the trapped charges can be read out by the XE SCM.

